REMARKS/ARGUMENTS

Claims 16-24, 26-28, and 31 remain pending in this application and stand rejected. Claims 16-24, 26-28, and 31 have been amended to clarify their respective languages and more fully define the scope of the inventions claimed therein. Claim 16 is further amended to include the limitations of claim 25. Support for these amendments can be found in the specification, for example, on pages 4-5.

Claims 16-27 and 31 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Publication 2003/0101307 ("Gemelli"). Applicant traverses these rejections. There is no disclosure in Gemelli of "a plurality of bus/communication protocols...", "presenting the subset of the plurality of bus/communication protocols to the system designer...." and "receiving a selection from the system designer...."

Gemelli discusses only one protocol, referred to as "COMMON BUS PROTOCOL", in paragraph 501, and reproduced below:

> "[0501] Now a protocol governing transactions through the COMMON-BUS is disclosed. This protocol will be named COMMON BUS PROTOCOL. The explanation starts with reference to FIG. 29 for introducing basic transactions. FIG. 29, which in turn refers to the previous FIG. 12 and FIG. 13 for COMMON-BUS wiring detail, differs from FIG. 13 mainly for the presence of an EXTERNAL BUS AGENT block connected to the main block DMI MAIN, through the EXTERNAL-BUS, and for the indication of three user macro-cells. Said three macro-cells are user MACRO-CELL A, user MACRO-CELL B, and user MACRO-CELL C, respectively connected to peripheral blocks DMI PERIPHERAL1, DMI PERIPHERAL2, and DMI PERIPHERAL3 of the distributed interface, via three Point-to-Point-Buses. In FIG. 29 Read/Write directions on both EXTERNAL-BUS and COMMON-BUS are indicated by arrows, respectively for the cases of block DMI MAIN master or slave."

Gemelli fails to teach "a plurality of bus/communication protocols". If the Examiner believes otherwise, he is requested to show where in Gemelli a plurality of bus protocols are shown. Since Gemelli does not teach "a plurality of bus/communication protocols," Gemelli also fails to teach "presenting the subset of the plurality of bus/communication protocols to the system designer...." and "receiving a selection from the system designer...." Applicant submits that, contrary to the Examiner's assertions, there is no disclosure in any of the Figures 2, 12-13, 15-17, 29, 31-38 and 40-43 of Gemelli of "presenting the subset of the plurality of bus/communication protocols to the system designer...." and "receiving a selection from the system designer...." as recited, in part, in amended claim 16.

Claims 16-24 and 26-27 also stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,721,830 ("Vorbach"). Applicant respectfully traverses these rejections. The Abstract and Figures 10-16 of Vorbach are cited by the Examiner as disclosing "comparing the plurality of bus/communication protocols of the component ports to identify a subset of the plurality of bus/communication protocols". Applicant traverses this rejection. The Abstract of Vorbach is reproduced below:

"A general bus system is provided which combines a number of internal lines and leads them as a bundle to the terminals. The bus system control is predefined and does not require any influence by the programmer. Any number of memories, peripherals or other units can be connected to the bus system (for cascading)."

There is not even a mention of "comparing the plurality of bus/communication protocols of the component ports to identify a subset of the plurality of bus/communication protocols" in this Abstract. Likewise, there is no mention of this claim limitation in any of Figures 10-16 and corresponding text of Vorbach, excerpts of which are reproduced below:

FIG. 10a shows the interconnection of two units (DFPs, FPGAs, DPGAs, etc.) (1001) linked together via the E-BUS (1002).

FIG. 10b shows the interconnection of a number of units (DFPs, FPGAs, DPGAs, etc.) (1001) via the E-BUS (1002).

FIG. 10c shows the interconnection of a number of units (DFPs, FPGAs, DPGAs, etc.) (1001) via the E-BUS (1002)....

FIG. 10d shows the interconnection [of a] unit (DFP, FPGA, DPGA, etc.) (1001) to a memory unit or a memory bank (1003) via the E-BUS (1002).

FIG. 10e shows the interconnection [of a] unit (DFP, FPGA, DPGA, etc.) (1001) to a peripheral device or a peripheral group (1004) via the E-BUS (1002).

FIG. 10f shows the interconnection [of a] unit (DFP, FPGA, DPGA, etc.) (1001) to a memory unit or a memory bank (1003) and to a peripheral device or a peripheral group (1004) via the E-BUS (1002).

FIG. 10g shows the interconnection [of a] unit (DFP, FPGA, DPGA, etc.) (1001) to a memory unit or a memory bank (1003) and to a peripheral device or a peripheral group (1004) plus another unit (DFP, FPGA, DPGA, etc.) (1001) via the E-BUS (1002).

FIG. 11 shows the architecture of the EB-REG....

FIG. 12 shows an example embodiment using a standard bus system RAMBUS (1203).....

FIG. 13 shows an example of implementation of an IO and memory bus system....

FIG. 14 shows an example bus IO unit....

FIG. 15a shows the address generator....

FIG. 15b shows a modification of the address generator from FIG. 15a.....

FIG. 15c shows the sequence in the state machine and the pattern of memory access by the address generator shown in FIG. 15b. ....

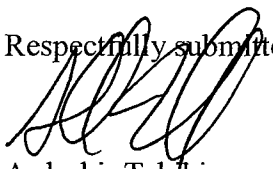
FIG. 16 shows the interaction of multiple segments in indirect addressing....

In column 5, Vorbach mentions that "any one of a number of conventional protocols may be implemented". However, there is no teaching or suggestion in Vorbach of " presenting the subset of the plurality of bus/communication protocols....and receiving a selection...", as recited, in part, in claim 16. Moreover, even though Vorbach mention that "any one of a number of conventional protocols may be implemented", there is no disclosure that the implemented protocol is carried out as a result of the "comparing the plurality of bus/communication protocols of the component ports to identify a subset of the plurality of bus/communication protocols". Vorbach fails to teach or suggest claims 16.

Claim 16 also stands rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,895,447 ("Brewer"). Claim 16 is amended to include the limitations of claim 25 and is allowable over Brewer. Applicant, however, submits that contrary to the Examiner's assertions, Brewer fails to teach "for each of the component ports, identifying a plurality of bus/communication protocols supported by the component port". As best understood, each device in Brewer communicates using only one protocol. Brewer fails to teach "a plurality of bus/communication protocols supported by the component port". Since Brewer does not teach "a plurality of bus/communication protocols supported by the component port," Brewer also fails to teach "presenting the subset of the plurality of bus/communication protocols to the system designer...." and "receiving a selection from the system designer....", as recited, in part, in claim 1. Claim 16 and its dependent claims 17-24, 26-28 and 31 are thus in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (650) 752-2424.

Respectfully submitted,



Ardeshir Tabibi
Reg. No. 48,750

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: (650) 326-2400
Fax: (650) 326-2422
AT:BCS:deh